A Low-power UHF Differential LNA in 0.35-μm SOI CMOS

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Abstract — **A low-power 435-MHz differential low-noise amplifier was implemented in a 0.35-μm Silicon On Insulator (SOI) CMOS process. This LNA is intended for use in a UHF receiver under development for deep space communications. The differential LNA has a measured noise figure of 3.25 dB, input 1-dB compression point of –14.18 dBm, input third-order intercept point of –5 dBm, and small-signal gain of 18.74 dB. Total power dissipation is 16.5 mW from a 2.5-V supply. LNA occupies a die area of 1 mm x 1.4 mm. This is the first UHF differential LNA implemented in an SOI CMOS process.**

I. Introduction

Extensive research has been conducted in the past years to realize full integration of CMOS receivers for wireless applications such as personal phones, Bluetooth, and wireless local area networks. Although there has been improvements in bulk CMOS processes for analog applications, analog circuits realized on bulk CMOS are susceptible to cross-talk, substrate noise, and Q factor degradation of integrated inductors due to the low-resistivity substrates [1]. Digital, mixed-signal, and RF integrated circuit designers have shown interest in the SOI CMOS process for low-power and high-speed applications. However, there is not a broad literature of SOI CMOS analog, mixed-signal or RF integrated circuit implementations covering different frequency ranges or applications.

Buried oxide layer between the bulk substrate and the active/passive layers is the fundamental difference that distinguishes SOI CMOS from bulk CMOS processes. This isolation layer eliminates many of the problems associated with the active device-substrate interactions.

Although there are many published CMOS LNA works above 900 MHz, very few studies have been reported at UHF frequencies. One of the challenges that fully integrated UHF LNA's pose is the low die area efficiency caused by the high inductor/capacitor values required to obtain resonances.

In this work, a low-power differential SOI CMOS LNA design is realized and the measured results are presented. The paper is organized as follows. Section 2 describes the RF characteristics of SOI CMOS processes in terms of active devices, integrated spiral inductors, and linearity. The differential LNA design is introduced in section 3. Measurement results are presented in section 4. Section 5 concludes the paper.

II. RF Characteristics of SOI CMOS

A. Active Device Features

Fig. 1 shows the cross-section of a typical SOI CMOS FET structure. SOI CMOS FET structure has many features common to bulk CMOS except an additional insulating layer under the thin active layer.

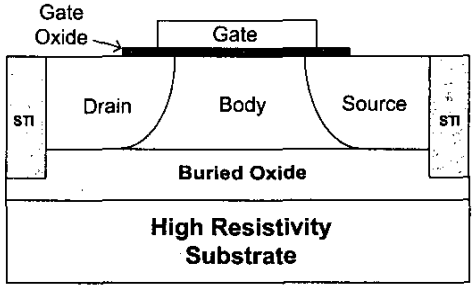

Fig. 1. Cross-section of an SOI CMOS FET structure

Unlike bulk CMOS, SOI CMOS has a high-resistivity substrate. The active silicon layer is isolated on all sides. Under the silicon is the buried oxide layer that provides isolation from the substrate. To the right and left of the active silicon layer are the shallow trench isolation (STI), which is similar to the STI isolation used in bulk CMOS. Gate oxide thickness is also comparable to the thickness in a typical CMOS process. High-resistivity substrate and buried oxide layer provide isolation that helps to decrease the substrate noise injected by noisy digital circuits into sensitive analog parts.

SOI CMOS provides a variety of advantages over bulk CMOS in terms of active device performance. SOI CMOS devices show high-speed performance even at low supply voltage levels (~1V). Low threshold voltages of SOI CMOS active devices allow low power designs. In SOI CMOS devices, junction capacitance is merely the buried oxide capacitance, which may be 4 to 7 times smaller than in bulk CMOS. Poly-to-substrate and metal-to-substrate capacitances are also lower. SOI CMOS is also highly

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attractive for deep space communication transceivers due to its radiation-hardness feature.

B. Transition Frequency, Noise Figure and Linearity in SOI CMOS

RF front-end of low-power wireless receiver applications has several performance requirements in terms of low-power dissipation, low noise figure and linearity. The noise figure and linearity of RF integrated-circuits are mainly affected by the Q-factor of passive elements, and the transistor characteristics.

The transition frequency of a MOSFET is given [1] by

$$f_T = \frac{g_m}{2\pi C_g} = \frac{1}{2\pi\left(C_{gs} + C_{gd} + C_p\right)}. \quad (1)$$

where g_m is the transconductance and C_g is the total capacitance appearing at the gate. C_g is composed of the internal gate-to-source capacitance (C_{gs}) , gate-to-drain capacitance (C_{gd}) and the additional capacitance that might come from interconnects or the input pads (C_p). The transition frequency is almost the same for comparable MOS transistors in bulk CMOS or SOI CMOS processes.

Thermal noise sets the sensitivity (minimum detectable signal power) of a receiver RF front-end. The achievable minimum noise figure for SOI CMOS transistors is expressed [1] by

$$NF_{\min} \cong 10\log\left(1 + 2\sqrt{R_n G_u}\right). \quad (2)$$

where R_n and G_u are the equivalent input noise resistance and conductance, respectively. R_n and G_u are expressed as

$$R_n \cong R_g + r_i + \frac{\gamma g_{do}}{g_m^2} + \left(\frac{g_{mb}}{g_m}\right)^2 \frac{R_{bb}}{1+\omega^2\cdot\tau_d^2}. \quad (3)$$

$$G_u \cong \frac{\gamma g_{d0}}{|h_{21}|^2} + \frac{g_{mb}^2 R_{bb}}{\left(1+\omega^2\tau_d^2\right)\cdot|h_{21}|^2} + \omega^2 C_{po}^2 \cdot \left(\frac{R_g + r_i + R_{pb}}{1+\omega^2\tau_a^2}\right). \quad (4)$$

where $\tau_d \cong C_b \cdot R_{bb}$, $\tau_a = C_g R_g + \left(C_{pb} + C_{po}\right)R_{pb}$, $|h_{21}|$ is the short-circuit current gain, g_{do} is the zero-bias channel conductance, g_{mb} is the back-gate effect, channel substrate transconductance, R_{bb} is the body or substrate resistance, and C_b is the body-channel capacitance. The inversion layer charging resistor is $r_i \sim 1/5g_m$. Gate resistance R_g is smaller than r_i for transistors with salicided gate multifinger layout. The first term in (4) represents the channel thermal noise, the second term indicates the body resistance induced noise coupled through the back-gate effect. The third term is the substrate thermal noise coupled through the pad or interconnects. C_{po} is the pad-substrate capacitance of the dielectric stack layer, R_{pb} models the substrate resistance [1].

Third order intermodulation (*IM3*) is a result of the nonlinear current-voltage characteristics of transistors. This nonlinearity represents a transconductance changing as a function of the input signal power. Adjacent channel interferers start distorting the carrier signal as the input AC power level increases. Input third order intercept point is defined as the cross-section point of the lines extrapolated from the linear sections of the first order and third order signals appearing at the output of the amplifier. *IP3* is limited by the reduced breakdown voltage and the low-frequency, impact ionization-induced output kink [2] which causes a nonlinear output conductance.

SOI CMOS transistors suffer from the transconductance nonlinearity like the bulk CMOS transistors but it is not effected by the voltage-dependency of drain capacitance due to the presence of the buried oxide layer.

C. Integrated Inductors

Performance of passive devices in SOI CMOS process is better than the devices in bulk CMOS. There have been reports on integrated spiral inductors built in SOI CMOS processes having higher quality factors and higher self-resonance frequencies than their bulk CMOS counterparts [3]. Examples demonstrating the performance of high-Q SOI inductors can be found in [4].

Spiral inductors and bonding pads, which usually occupy large metal area, allow the substrate noise to couple into the circuitry and get amplified by the transistor action. High-resistivity SOI substrate suppresses the losses from bonding pads, integrated spiral inductors and noise coupled through the substrate. Reduced substrate noise coupling makes SOI CMOS particularly attractive for integration of RF and digital circuits on the same substrate. High resistivity bulk in the SOI CMOS also offers the possibility of improving passive components Q-factor.

III. The Design of the Differential LNA

Low-noise amplifiers are the major blocks that determine the overall noise figure and therefore the sensitivity of a receiver chain. The low-noise amplifier designed in this work is a differential one with source degeneration as shown in Fig.2. Differential topology is adopted due to the inherent immunity to substrate and supply noise. The inductor L_s provides a real part to the input impedance at the gates of N1 and N2. That real part which is in the order of 100-150Ω is reduced to lower values due to the presence of the parasitic capacitance impressed by the pads and ESD protection diodes. The input impedance is then matched to 50 Ω through off-chip matching elements. The equal size transistor pairs N1, N3 and N2, N4 constitute a cascode configuration that lowers the Miller capacitance preventing the input impedance degradation. Cascode configuration also provides increased input-output isolation. Drain inductor L_d is

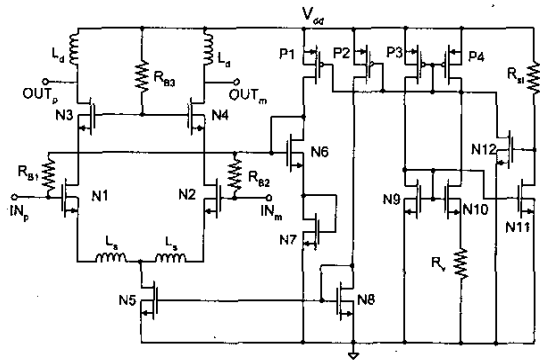

Fig. 2. The differential LNA schematic.

TABLE I.
ELEMENTS OF THE LNA

N1-N4	350/0.35 μm	N12	45/1.55 μm
N5	400/1.2 μm	P1	60/1.55 μm
N6-N7	75/1.2 μm	P2-P4	120/1.55 μm
N8	30/1.2 μm	R_{B1},R_{B2}	60 kΩ
N9	30/0.5 μm	R_{B3}	4 kΩ
N10	240/0.5 μm	R_v	600 Ω
N11	30/0.5 μm	R_{st}	20 kΩ

adjusted such that it will resonate with the total parasitic drain capacitances of N3 and N4 at 435 MHz. Transistors N1-N4 are chosen as 350-μm wide although this is not the noise optimum widths at 435 MHz according to [5]. Optimum width is not selected since low overdrive voltage is not acceptable for proper biasing of the LNA.

P-well resistors R_{B1}, R_{B2}, and R_{B3} provide the bias voltages for the input and output transistors' gates. PMOS transistors P1-P4 and NMOS transistors N5-N10 make up a constant-g_m bias circuit to provide the DC current to the LNA core through N5. The value of this current is controlled by the off-chip resistor R_v. NMOS transistors N11-N12 and R_{st} are for the startup of the constant-g_m bias circuit. Table 1 shows the values of the LNA components. Bodies are tied to the transistor sources which offers small threshold voltage levels (~ 0.65 V). Use of multifinger gates in the layout results in a significant decrease in the gate electrode resistance which directly effects the RF performance. All the simulations were done using SpectreRF.

IV. Measured Results

Figures 3 and 4 show the measured small-signal gain, input reflection and the input-output isolation. The LNA provides a small-signal gain of 18.74 dB at 435 MHz. Input return loss is 11.76 dB and the input-output (reverse) isolation is 20.83 dB. The noise figure as a function of frequency is shown in Fig. 5. The noise figure at 435 MHz is 3.25 dB. This low noise figure is a result of both the UHF operation and the lower minimum achievable noise figure of the SOI CMOS transistors. Fig. 6 shows the small-signal gain of the amplifier as a function of the input RF power. Small-signal gain drops by 1 dB when the input RF power level reaches -14.18 dBm, which is the input 1-dB compression point of the LNA.

The two-tone analysis is done by applying two RF signals at the input of the LNA at the frequencies of 435 MHz and 440 MHz. Signal power is varied and the powers of the fundamental component (435MHz) and the intermodulation component (445 MHz) is measured at the output. Fig. 7 shows the two-tone characteristics of the LNA. Input IP3 point is at -5 dBm and the output IP3 is at +10 dBm. Total power dissipation is 16.5 mW from a 2.5V supply.

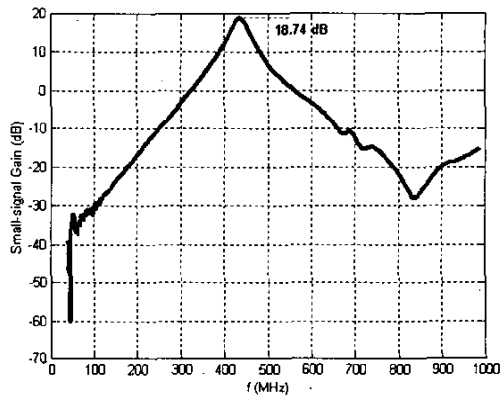

Fig. 3. LNA small-signal gain

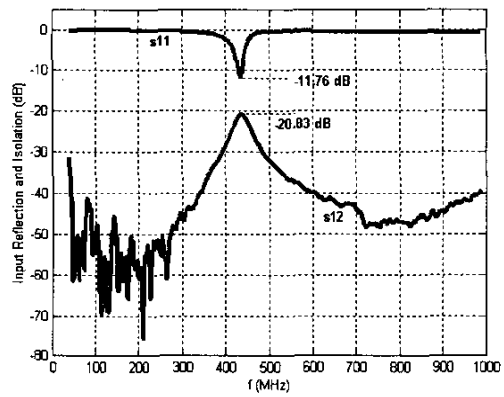

Fig. 4. Input reflection and reverse isolation

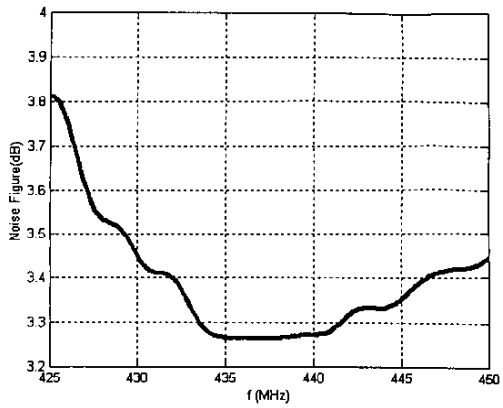

Fig. 5. Noise figure of the LNA

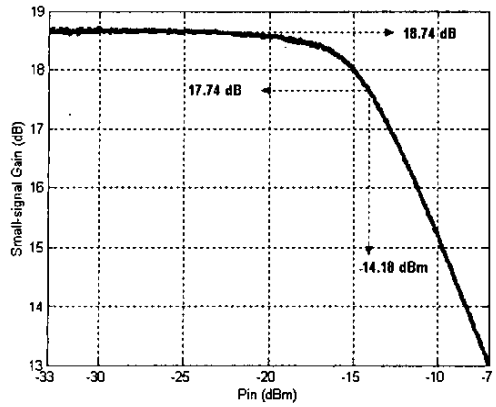

Fig. 6. Small-signal gain as a function of input power

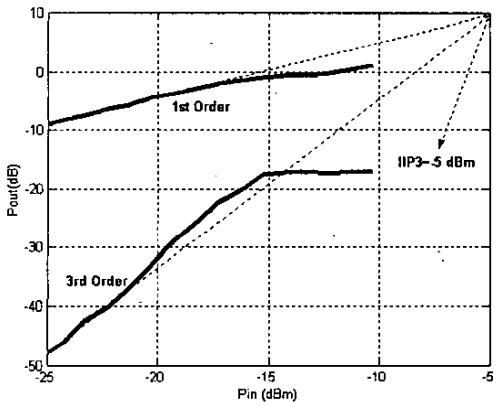

Fig. 7. Two-tone characteristics

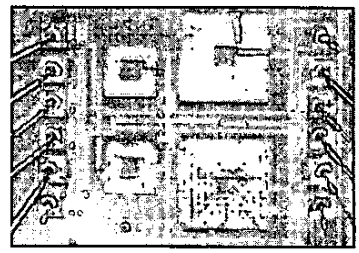

Fig. 8. Microphotograph of the wirebonded SOI LNA chip

Microphotograph of the SOI CMOS LNA is shown in Fig. 8. Input and output pads are ESD protected with the reverse-biased junction diodes connected between the signal and the bias pads. Total chip area is 1 mm x1.4 mm.

V. CONCLUSION

A low-power differential LNA has been realized using a 0.35-μm SOI CMOS process. RF characteristics of SOI CMOS transistors and spiral inductors have also been elaborated. Measurement results show that designing high performance low-noise amplifiers is possible with low-power dissipation in SOI CMOS technology. This and other arising RF integrated circuit examples based on SOI CMOS technology offers promise for future applications.

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